REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 3 through 11, 13 through 21, 23 through 28, 30 through 34, 38, 40 through 42, 44, and 45 remain in this case. Claims 1, 6, 16, 21, 26, 33, and 38 are amended. Claims 2, 12, 22, 29, 35 through 37, 39, and 43 were previously canceled.

Claims 1, 3 through 7, 9, 11, 13 through 17, 19, 21, 23 through 26, 28, 30, 31 through 33, 35, 38, 40, 42, and 44 were rejected under §102(e) as anticipated by the Smith reference[1]. Claims 3, 13, 23, 30, 36, 40, and 43 were rejected under §103 as unpatentable over the Smith reference in view of Applicants' admitted prior art. Claims 9, 10, 19, 20, 27, 34, 37, 41, and 45 were rejected under §103 as unpatentable over the Smith reference in view of the Kramer reference[2], and claims 4, 5, 7, 8, 14, 15, 17, 18, 24, 25, 31, and 32 were rejected under §103 as unpatentable over the Smith reference in view of the Bruce et al. reference[3].

Claim 1 is amended to overcome the rejection to it and its dependent claims. Amended claim 1 now expressly recites that non-volatile memory is comprised of a plurality of blocks in an array formed on a semiconductor substrate.[4] The method of claim 1 now also recites the writing of a first block in this array with data encoded according to a first error detection algorithm, responsive to the indicator for that first block meeting a criterion, and the writing of a second block in that same array, and thus on the same semiconductor substrate, data encoded according to a second error detection algorithm responsive to the indicator for that second block not meeting the criterion. Support for this amendment to claim 1 is clearly present in the specification, as noted above, and as such no new matter is presented by this amendment.

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[1] U.S. Patent No. 6,961,890 B2, issued November 1, 2005 to Smith, from an application filed August 16, 2001.
[2] U.S. Patent No. 6,182,239 B1, issued January 20, 2001 to Kramer.
[3] U.S. Patent No. 5,956,743, issued September 21, 1999 to Bruce et al.
[4] *See, e.g.*, specification of S.N. 10/678,893, at page 11, lines 25 through 28; page 12, lines 4 through 5 and lines 24 through 27.

Applicants respectfully submit that amended claim 1 and its dependent claims are novel and patentably distinct over the Smith reference and the other references of record in this case, because the Smith reference fails to disclose a method in which a first block within a memory array is written with data encoded according to a first error detection algorithm, and a second block within that same memory array is written with data encoded according to a second error detection algorithm, as required by amended claim 1.

The Smith reference is directed to the selection of an error correcting code based on a "fundamental error rate" for a given memory device, considered as a whole. The reference expressly teaches that the data structure of its memory may be associated with one or more integrated circuits "within which it is reasonable to assume that the fundamental error rate will be generally homogeneous".[5] As such, the Smith reference applies a single error correcting code over an entire memory array; while the reference discloses multiple "dividers" representing the error correcting codes of different weight, these alternative dividers "are alternatives to the first divider 206, and [ ] only one divider may be used at a given time".[6] The application of one error correcting code over the memory array as a whole, according to the Smith reference, is also apparent considering that the selection of the error correcting code is based on the parameters of technology type and use application,[7] both of which apply to the memory array as a whole and not to individual blocks within the array.

Accordingly, Applicants submit that the Smith reference does not disclose the writing of data encoded using a first error detection algorithm into a first block of a memory array, in combination with the writing of data encoded using a second error detection algorithm into a second block of that same memory array, as required by amended claim 1. Applicants therefore submit that amended claim 1 and its dependent claims are all novel over the Smith reference.

Applicants further respectfully submit that amended claim 1 and its dependent claims are also patentably distinct over the Smith reference in view of the other prior art of record in this

[5] Smith, *supra,* column 4, lines 18 through 22.
[6] *Id.,* at column 4, lines 29 through 31.
[7] *Id.,* at column 6, line 39 through column 7, line 2; column 7, line 57 through 64; column 8, lines 32 through 46.

case, because the combined teachings of the references fall short of the requirements of amended claim 1.

While the admitted prior art states that 1-bit and 2-bit ECC algorithms are known, that admitted prior art does not include any prior knowledge regarding encoding data for one block in an array according to one ECC algorithm, and encoding data for another block in that same array according to a different ECC algorithm. The Kramer and Bruce et al. references also lack teachings in this regard, nor were these references asserted as providing such teachings.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the combination of these teachings in such a manner as to reach amended claim 1. As described in the specification,[8] the inventive method of claim 1 provides the important advantage of optimizing the error detection and correction coding within a memory array based on the reliability of the individual memory block being written. For example, if a given block has been subjected to relatively few erase cycles, a less robust error correction coding may be used so that more data may be stored in that block; on the other hand, if another block in that array is relatively worn because of a larger number of erase cycles, a more robust error correction coding can be used to improve the accuracy of the data stored in that block, while maintaining the less-robust coding in the first block to obtain more data storage. Nowhere do any of the applied references suggest the selection of error detection algorithms for blocks within a common memory array, as required by amended claim 1. And as such, the prior art nowhere suggests modifying the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 1.

For these reasons, Applicants submit that amended claim 1 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

Claim 6 is also amended to overcome the rejection. Amended claim 6 now recites that the non-volatile memory comprises a plurality of blocks in an array formed on a semiconductor

[8] Specification, *supra*, page 8, lines 12 through 29.

substrate,[9] and further recites the repeating of the identifying, obtaining, determining, encoding, and writing steps for another block in the array, such that, as a result of the repeating step, a first block in the array stores data encoded according to the first algorithm and a second block in that array stores data encoded according to the second algorithm.[10] Given the support for this amendment to claim 6 in the specification, as noted, Applicants submit that no new matter is presented by this amendment.

Applicants respectfully submit that amended claim 6 and its dependent claims are novel and patentably distinct over the Smith reference and the other references of record in this case. The Smith reference fails to disclose a method in which the repeated writing of blocks in a memory array can result in a first block within a memory array storing data encoded according to a first error detection algorithm, and in a second block within that same memory array storing data encoded according to a second error detection algorithm, as required by amended claim 6.

As discussed above, the Smith reference is directed to the writing of data in a non-volatile memory device, considering the "fundamental error rate" of the memory device, considered as a whole. This consideration of the memory device as a whole, rather than on a block-by-block basis within a memory array, is evident from the statement in the Smith reference that "it is reasonable to assume that the fundamental error rate will be generally homogeneous" within its memory data structures.[11] The reference teaches using that assumption to apply a single error correcting code over an entire memory array.[12] Furthermore, the Smith reference teaches using the parameters of technology type, and use application, both of which apply to entire memories and not to individual blocks within a memory, to select the error correcting code.[13]

Accordingly, Applicants submit that the Smith reference does not disclose the repeated determining of whether an indicator associated with a memory block is less than a threshold value, to select either a first error detection algorithm or a second error detection algorithm to

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[9] *See, e.g.,* specification, *supra,* at page 11, lines 25 through 28; page 12, lines 4 through 5 and lines 24 through 27.
[10] Specification, *supra,* page 15, lines 20 through 25.
[11] Smith, *supra,* column 4, lines 18 through 22.
[12] *Id.,* at column 4, lines 29 through 31 ("only one divider may be used at a given time").
[13] *Id.,* at column 6, line 39 through column 7, line 2; column 7, line 57 through 64; column 8, lines 32 through 46.

encode the data to be written, much less resulting in a first block of the array storing data encoded according to the first algorithm and a second block of that array storing data encoded according to a second error detection algorithm, as claimed. Applicants therefore submit that amended claim 6 and its dependent claims are all novel over the Smith reference.

Applicants further respectfully submit that amended claim 6 and its dependent claims are also patentably distinct over the Smith reference in view of the other prior art of record in this case, because the combined teachings of the references fall short of the requirements of amended claim 6 and because there is no suggestion from the art to modify these teachings so as to reach the claim.

The other prior art does not make up the shortfall of the Smith reference relative to amended claim 6. As discussed above, the admitted prior art does not include any prior knowledge regarding the encoding of data for one block in an array according to one ECC algorithm, and the encoding of data for another block in that same array according to a different ECC algorithm. The Kramer and Bruce et al. references also lack teachings in this regard, nor were these references asserted as providing such teachings.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the combination of these teachings in such a manner as to reach amended claim 6. Similarly as discussed above relative to claim 1, the method of claim 6 provides the important advantage of optimizing the error detection and correction coding within a memory array using reliability information on a block-by-block basis, rather than over the memory array as a whole. This block-by-block determination optimizes the usage of the memory – increasing the data capacity (*i.e.,* with less error correction) for reliable blocks, and increasing the error correction (*i.e.,* reducing the data capacity) for less reliable blocks. Because none of the applied references suggest the selection of error detection algorithms for blocks within a common memory array, the prior art lacks any suggestion to modify the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 6.

For these reasons, Applicants submit that amended claim 6 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

Independent claim 16 is also amended to overcome the rejection. Claim 16 is directed to a method for reading data stored in a non-volatile memory, where the memory comprises a plurality of blocks in an array formed on a semiconductor substrate.[14] The claim also recites the step of identifying one of the plurality of blocks from which data is to be read, obtaining an indicator from that block, determining whether the indicator is less than a threshold value; if so, the data from that block is decoded using a first error detection algorithm, and if not, the data is decoded using a second error detection algorithm that has a higher error detection capability. No new matter is presented by this amendment, considering its clear support in the specification, as discussed above.

Applicants submit that independent claim 16 and its dependent claims are novel and patentably distinct over the Smith reference and the other prior art of record in this case. Nowhere does the Smith reference, nor any of the other prior art, disclose reading data from one of a plurality of blocks from a memory array formed at a common semiconductor substrate, comprising decoding the data according to a first or a second error detection algorithm, depending on whether an indicator of the number of times that the block has been erased is less than a threshold value, as required by amended claim 16.

As discussed above, the Smith reference is directed to the writing of data in a non-volatile memory device, and thus the reading back of that data, using an error correction code that is selected by considering the "fundamental error rate" that is assumed to "be generally homogeneous" over the entire data structure of the memory device.[15] Based on this assumption, and based on parameters such as technology type and the application for which the memory devices is to be used, the Smith reference teaches the selecting of a single error correcting code, for the entire memory array, to be used for encoding data written to, and decoding data read

[14] *See, e.g.,* specification, *supra,* at page 11, lines 25 through 28; page 12, lines 4 through 5 and lines 24 through 27.
[15] Smith, *supra,* column 4, lines 18 through 22.

from, that array.[16] Accordingly, Applicants submit that the Smith reference does not disclose and cannot suggest the reading of data from individual blocks within the memory by obtaining an indicator associated with that individual block, and decoding the data according to a first error detection algorithm or a second error detection algorithm, depending on whether the indicator is less than a threshold value. Rather, according to the Smith reference, any and all blocks of the memory will be read using the same error correction code, namely whichever error correction code was selected for that memory device. Applicants therefore submit that amended claim 16 and its dependent claims are all novel over the Smith reference.

Applicants further respectfully submit that amended claim 16 and its dependent claims are also patentably distinct over the Smith reference in view of the other prior art of record in this case, because the combined teachings of the references fall short of the requirements of amended claim 16 and because there is no suggestion from the art to modify these teachings so as to reach the claim.

As discussed above, the prior art other than the Smith reference does not make up the shortfall of the Smith reference, as measured relative to amended claim 16. As discussed above, the admitted prior art does not include any prior knowledge regarding the decoding of data from different blocks in a memory array using different ECC algorithms. Nor do the Kramer and Bruce et al. references provide teachings in this regard.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the combination of these teachings in such a manner as to reach amended claim 16. Similarly as discussed above relative to the other claims in this case, the method of claim 16 provides the important advantage of optimizing the error detection and correction coding within a memory array using reliability information on a block-by-block basis, rather than over the memory array as a whole. This block-by-block determination optimizes the usage of the memory – increasing the data capacity (*i.e.,* with less error correction) for reliable blocks, and increasing the error correction (*i.e.,* reducing the data capacity) for less reliable blocks. Because

[16] *Id.*, at column 4, lines 29 through 31 ("only one divider may be used at a given time").

none of the applied references suggest that different error detection algorithms may be applied to different blocks within a common memory array, the prior art lacks any suggestion to modify the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 16.

For these reasons, Applicants submit that amended claim 16 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

Independent claims 21 and 26 are each also amended in a similar manner as claims 1 and 6, to overcome the rejection and for clarity. Amended claims 21 and 26 each now recite a non-volatile memory array that is formed on a semiconductor substrate.[17] No new matter is presented by this amendment to claims 21 and 26, and entry of this amendment is requested.

Applicants respectfully submit that amended claim 21 and its dependent claims, and claims 26 and its dependent claims, are novel and patentably distinct over the Smith reference and the other prior art of record in this case.

As discussed above relative to claims 1 and 6, Applicants submit that the Smith reference fails to disclose code devices for identifying one of a plurality of blocks in a memory array formed on a semiconductor substrate, code devices for obtaining an indicator associated with that block having a value indicative of the reliability of the block, and code devices for encoding data using a first error detection algorithm or a second error detection algorithm, based on the indicator meeting or not meeting a criterion (in claim 21), or indicating that the number of times that the identified block has been erased is less than a threshold value (in claim 26). It is apparent from each of claims 21 and 26 that, because these code devices are recited as operating on individual blocks by using either a first or second error detection algorithm based on an indicator for each individual block, different blocks in the same memory array can be encoded according to different error detection algorithms.

[17] *See, e.g.,* specification, *supra,* at page 11, lines 25 through 28; page 12, lines 4 through 5 and lines 24 through 27.

In contrast, the Smith reference encodes the data that it writes according to an algorithm selected for the memory device considered as a whole. This is evident from the Smith reference stating that "it is reasonable to assume that the fundamental error rate will be generally homogeneous" for a given memory data structure,[18] and teaching the use of this assumption to apply the same error correcting code to an entire memory array.[19] The parameters disclosed in the Smith reference, as determining which error correction code to use, include the parameters of technology type and application of the memory, both of which apply to entire memories and not to individual blocks within a memory.[20]

Accordingly, Applicants submit that the Smith reference does not disclose code devices for encoding data to be written to one block of a plurality of blocks in an array, according to a first error detection algorithm or a second error detection algorithm, based on the relationship of an indicator for that block meeting or not meeting a criterion, as claimed by amended claim 21, or being less than a threshold value, as claimed by amended claim 26. Applicants therefore submit that amended claim 21 and its dependent claims, and amended claim 26 and its dependent claims, are novel over the Smith reference.

Applicants further respectfully submit that there is no suggestion from the art to combine the teachings, or to modify the combined teachings, of the Smith reference and those of the other prior art of record in this case in such a manner as to reach claim 21 or claim 26.

First, the other prior art does not make up the shortfall of the Smith reference relative to these claims. As discussed above, the admitted prior art does not include any prior knowledge regarding block-by-block decision circuitry to select one of multiple ECC algorithms for encoding data for individual blocks in an array. Nor do the Kramer and Bruce et al. references provide any teachings in this regard.

Secondly, Applicants respectfully submit that there is no suggestion from the prior art to modify these teachings, if combined, in such a manner as to reach amended claim 21 or claim 26.

[18] Smith, *supra,* column 4, lines 18 through 22.
[19] *Id.,* at column 4, lines 29 through 31 ("only one divider may be used at a given time").

Similarly as discussed above relative to claims 1 and 6, the claimed systems provide the important advantage of optimizing the error detection and correction coding within a memory array using reliability information on a block-by-block basis, rather than over the memory array as a whole. Both the data capacity and the error rate of the memory are optimized, because the more robust error detection is applied only to blocks within the memory array that indicate less reliability, based on their individual block indicators. Because none of the applied references suggest the selection of error detection algorithms for individual blocks within a common memory array, the prior art lacks any suggestion to modify the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 21, or in such a manner as to reach Applicants' invention of amended claim 26.

For these reasons, Applicants submit that amended claim 21 and its dependent claims, and amended claim 26 and its dependent claims, are all novel and patentably distinct over the prior art of record in this case.

Independent claim 33 is similarly amended as claim 16, to now be directed to a memory system comprised of a non-volatile memory array formed on a semiconductor substrate and including a plurality of blocks, code devices for obtaining an indicator associated with an identified block that indicates a number of times the block has been erased, and code devices for determining whether the indicator for that block is less than a threshold value. The system further includes code devices for decoding the data from the block according to a first error detection algorithm if the indicator is less than a threshold value, and code devices for decoding the data according to a second, more robust, error detection algorithm otherwise. As discussed above for the other amended claims, no new matter is presented by this amendment.

Applicants submit that independent claim 33 and its dependent claims are novel and patentably distinct over the Smith reference. Nowhere does the Smith reference, nor any of the other prior art, disclose any circuitry that obtains an indicator from an individual block and determines, based on that indicator, whether data to be read from that block is decoded according

[20] *Id.*, at column 6, line 39 through column 7, line 2; column 7, line 57 through 64; column 8, lines 32 through 46.

to either of a first or a second error detection algorithm. Instead, as discussed repeatedly above, the Smith reference is directed to the writing and reading of data in a non-volatile memory device, using an error correction code that is selected for the entire memory device assuming a "generally homogenous fundamental error rate" over the entire data structure of the memory device.[21] The particular error correction code is selected for the entire memory device based on this assumption, and based on parameters such as technology type and the application of the memory device.[22] Accordingly, Applicants submit that the Smith reference does not disclose and cannot suggest the decoding of data from an individual block of a memory array according to a first error detection algorithm or a second error detection algorithm, depending on whether the indicator is less than a threshold value. Instead, the Smith reference teaches only that any and all blocks of the memory will be decoded using the same error correction code, namely whichever error correction code was selected for that memory device. Applicants therefore submit that amended claim 33 and its dependent claims are all novel over the Smith reference.

Applicants further respectfully submit that amended claim 33 and its dependent claims are also patentably distinct over the Smith reference in view of the other prior art of record in this case, because the combined teachings of the references fall short of the requirements of amended claim 33 and because there is no suggestion from the art to modify these teachings so as to reach the claim.

As discussed above, the prior art other than the Smith reference does not disclose the features of amended claim 33 that are not taught by the Smith reference. Specifically, neither the admitted prior art, nor the Kramer reference, nor the Bruce et al. reference, indicates any prior knowledge of the decoding of data from different blocks in a given memory array using different ECC algorithms.

Nor is there is suggestion from the prior art to modify the combination of these teachings in such a manner as to reach amended claim 33. Similarly as discussed above relative to the other claims in this case, the system of claim 33 provides the important advantage that its data

[21] Smith, *supra,* column 4, lines 18 through 22.
[22] *Id.*, at column 4, lines 29 through 31 ("only one divider may be used at a given time").

storage capacity and error detection capabilities are optimized by decoding the individual blocks according to error detection algorithms selected for each block individually, rather than over the memory array as a whole. Because none of the applied references suggest that different error detection algorithms may be applied to different blocks within a common memory array, the prior art lacks any suggestion to modify the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 33.

For these reasons, Applicants submit that amended claim 33 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

Claim 38 is also amended to overcome the rejection. Amended claim 38 now requires a non-volatile memory array formed on a semiconductor substrate, where the array includes a plurality of blocks. Claim 38 also further recites that repeated operation of the means that obtain an indicator, and the means that encode data using a first or a second error detection algorithm for a given block responsive to whether the indicator meets a criterion, results in a first block in the array storing data encoded according to the first algorithm and a second block in that array storing data encoded according to the second algorithm.[23] Given the support in the specification for this amendment to claim 38, Applicants submit that no new matter is presented by this amendment.

Applicants respectfully submit that amended claim 38 and its dependent claims are novel and patentably distinct over the Smith reference and the other references of record in this case. The Smith reference fails to disclose a method in which the repeated operation of its circuitry on blocks in a memory array can result in a first block within a memory array storing data encoded according to a first error detection algorithm, and in a second block within that same memory array storing data encoded according to a second error detection algorithm, as claimed.

Rather, the Smith reference is directed to the writing of data in a non-volatile memory device, with an error correction code selected based on the "fundamental error rate" of the memory device, considered as a whole because "it is reasonable to assume that the fundamental

[23] Specification, *supra*, page 15, lines 20 through 25.

error rate will be generally homogeneous" within a memory data structure.[24] Indeed, the Smith reference teaches using the parameters of technology type, and use application, both of which apply to entire memories and neither of which can apply to individual blocks within a memory array, to select its error correcting code.[25]

Accordingly, Applicants submit that the Smith reference does not disclose the recited means in amended claim 38, which operate on an individual block at a time, and that result of which is a first block of the array storing data encoded according to the first algorithm and a second block of that array storing data encoded according to a second error detection algorithm, as claimed. Applicants therefore submit that amended claim 38 and its dependent claims are all novel over the Smith reference.

Applicants further respectfully submit that amended claim 38 and its dependent claims are also patentably distinct over the Smith reference in view of the other prior art of record in this case, because the combined teachings of the references fall short of the requirements of amended claim 38 and because there is no suggestion from the art to modify these teachings so as to reach the claim.

The other prior art does not make up the shortfall of the Smith reference relative to amended claim 38. As discussed above, the admitted prior art does not include any prior knowledge regarding the encoding of data for one block in an array according to one ECC algorithm, and the encoding of data for another block in that same array according to a different ECC algorithm. The Kramer and Bruce et al. references also lack teachings in this regard, nor were these references asserted as providing such teachings.

Nor is there suggestion from the prior art to modify the combination of these teachings in such a manner as to reach amended claim 38. Similarly as discussed above relative to claims 1, 6, and the other independent claims, the system of claim 38 provides the important advantage of optimizing the error detection and correction coding within a memory array using reliability

[24] Smith, *supra,* column 4, lines 18 through 22.
[25] *Id.*, at column 6, line 39 through column 7, line 2; column 7, line 57 through 64; column 8, lines 32 through 46.

information on a block-by-block basis, rather than over the memory array as a whole. This block-by-block determination optimizes the usage of the memory – increasing the data capacity (*i.e.,* with less error correction) for reliable blocks, and increasing the error correction (*i.e.,* reducing the data capacity) for less reliable blocks. Because none of the applied references suggest that different error detection algorithms may be used on different blocks within a common memory array, the prior art lacks any suggestion to modify the teachings of the Smith and other references in such a manner as to reach Applicants' invention of amended claim 38.

For these reasons, Applicants submit that amended claim 38 and its dependent claims are not only novel, but are patentably distinct over the prior art of record in this case.

The prior art cited as pertinent has been considered, but is not felt to come within the scope of the claims in this case.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,
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